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MVIO Delay Compact HD/SD Video/Audio Time-Delay

User manual V1.1

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Content

MVIO DELAY
Compact HD/SD Video/Audio Time-Delay

I MVIO Delay Description

MVIO DELAY provides effective video/audio delay for HD or SD signal in a 1U half chassis. Through it one HD/SD-SDI video/audio signal can output after overall delay. MVIO DELAY supports balanced signal amplification, frame synchronization and V/A relative delay. The delay time is up to 20 seconds. The adjustment range is ±15 frames. It supports PAL, NTSC and tri-level sync signal. The front panel supports shortcut-key quick switch before or after delay.

II MVIO DELAY Output, Input and Functions

2.1 MVIO Delay Output and Input

1. MVIO DELAY

Input: 1 HD/SD digital signal

1 BB signal, supports PAL, NTSC and tri-level sync signal.

Input: 3 HD/SD digital signals

Function control: SDI signal delay supports up to 20s

Video/Audio relative delay adjustment supports ±15 frames.

2. HD/SD Signals Supported

SD: 525i60, 625i50

HD: 720p60, 720p59.94, 720p50, 1080i60,1080i59.94,

1080i50, 1080p30, 1080p29.97, 1080p25

MVIO DELAY supports frame sync, and H-phase is adjustable. The sync signal supported by outside phase lock:

Format Type	625i50	720p50	1080i50	1080p25	525i60	720p59.94
PAL-BB	√	√	√	√	----	----
NTSC-BB	----	----	----	----	√	√
Tri-level	√	√	√	√	√	----

Format Type	1080i59.94	1080p29.97	720p60	1080i60	1080p30	
PAL-BB	----	----	----	----	----	
NTSC-BB	√	√	----	----	----	
Tri-level	----	----	√	√	√	

Notes: √ --support; ---- --not support

III MVIO Delay Panels

3.1 MVIO Delay front panel
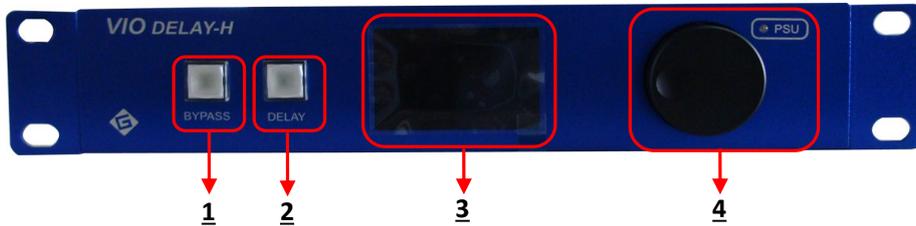
1. BYPASS button: Quickly switch to the original output signal. press the button, it show yellow which means current output signal is the original signal before delay.

    Tips: in this status, only the H phase's setting of output signal is valid, both A/V relative delay adjustment and A/V overall delay are invalid. That is there is no delay for input and output signals.

2. DELAY button: Quickly switch to the delay signal. press the button, it show yellow which means current output signal is the signal after delay.

    Tips: in this status, the H phase's setting of output signal, A/V relative delay adjustment and A/V overall delay are all valid.

    When A/V relative delay adjustment is set as 0F0H, this module is invalid and has no influence on video delay. Only H phase setting and A/V overall delay is available. For instance, A/V relative delay adjustment is set as 0F0H, A/V overall delay is 0S1F, the output image delays 1 frame.

    If A/V relative delay adjustment isn't set as 0F0H, it delays 15 frames automatically, and then it is accumulated to A/V overall delay.

    If A/V relative delay adjustment is set as 1F0H, A/V overall delay is 0S1F, the output image delays 16 frames.

3. LCD Menu Display: display the settings of inner detail functions Please refer to Function Menu Instruction.

4. Function knob and power indicator: the function knob works with menu, it is used for page up, page down, value choice and press it to confirm. Power indicator is used to indicating power status. Usually it shows blue.

3.2 MVIO Delay rear panel
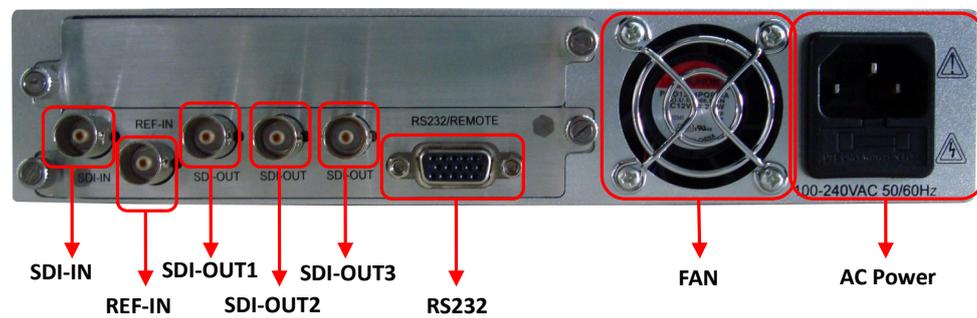
1. SDI-IN: HD/SD digital signal input interface. Input HD/SD digital signals.

2. REF-IN: sync signal input interface. Input sync signal.

3. SDI-OUT 1~3: HD/SD digital signal output interface.

4. RS232: RS232 serial port control interface. It is used in on-line inner FPGA upgrade (need the special software for upgrade).

IV MVIO DelayMenu and Control

4.1 MVIO Delay Menu

```
┌─────────────────────────────┐      ┌─────────────────────────┐
│ Delay Time：***S   ***F     │      │ Delay Time：            │
│  A/V Delay：A.adv  **F  **H │──┬── │       ***S   ***F       │
└─────────────────────────────┘  │   └─────────────────────────┘
                                 │   ┌─────────────────────────┐
                                 │   │ A/V Delay：             │
                                 ├── │   A.adv  ***F   ***H    │
                                 │   └─────────────────────────┘
                                 │   ┌─────────────────────────┐
                                 │   │ Genlock：               │
                                 ├── │                 INT     │
                                 │   └─────────────────────────┘
                                 │   ┌─────────────────────────┐
                                 │   │ H-Phase：               │
                                 ├── │             *** Pixels  │
                                 │   └─────────────────────────┘
                                 │   ┌─────────────────────────┐
                                 │   │ V-Phase：               │
                                 ├── │             *** Lines   │
                                 │   └─────────────────────────┘
                                 │   ┌─────────────────────────┐
                                 │   │ Version：               │
                                 ├── │              *.*.*      │
                                 │   └─────────────────────────┘
                                 │   ┌─────────────────────────┐
                                 │   │ FPGA-M Update：         │
                                 ├── │          Disable        │
                                 │   └─────────────────────────┘
                                 │   ┌─────────────────────────┐
                                 │   │ FPGA-S Update：         │
                                 └── │          Disable        │
                                     └─────────────────────────┘
```
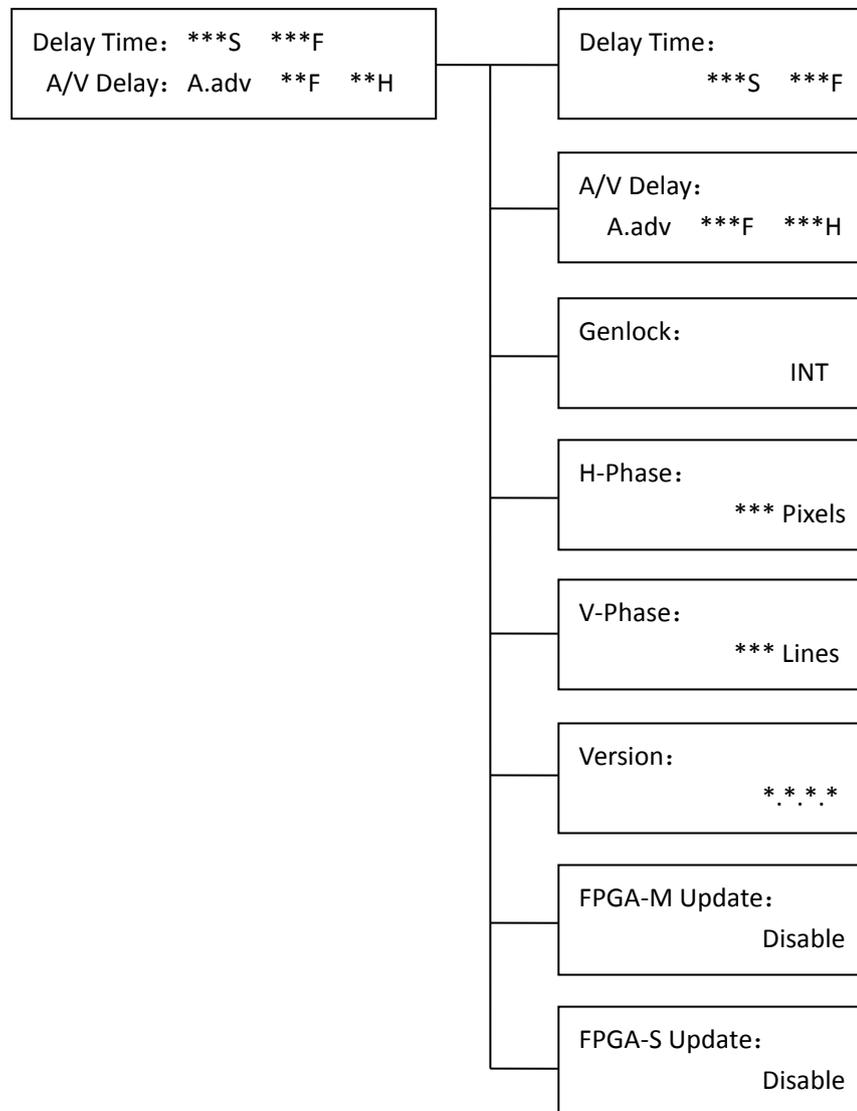
When menu is in standby, it displays the time of A/V overall delay and A/V relative delay. Inner setting details:

Delay Time:　setting of V/A signal overall delay. Units available are second (s) and frame (f). Second can be set up to 20s while frame can be set the maximum in 1 second (according to the frame frequency of input signal).

A/V Delay: setting of video/audio relative delay. Firstly, you can set audio in advance

(A.adv) or audio delay (A.dly), secondly set frame (F) and horizontal pixel as the delay unit. Besides, frame can be set up to 15, horizon can be set the maximum in 1 frame (according to the format of input signal).

Genlock: setting of input signal's phase lock. It can be set as external phase lock(EXT) and internal phase lock (INT).

H-Phase: setting of horizontal phase.

V-Phase: setting of vertical phase.

Version: show the version information of current internal programs.

FPGA-M Update: it is used for the setting of main FPGA upgrade. It can be set as Enable and Disable. When the inner main FPGA needs upgrade, please set it as Enable, then start upgrade with the special software. There will be a notice when upgrade successfully. If the equipment works well, this option must be set as Disable.

FPGA-S Update: it is used for the setting of subordinate FPGA upgrade. It can be set as Enable and Disable. When the inner subordinate FPGA needs upgrade, please set it as Enable, then start upgrade with the special software. There will be a notice when upgrade successfully. If the equipment works well, this option must be set as Disable.

Tips: when you upgrade the equipment, the menu will be still in current page whether if the setting of FPGA-M or FPGA-S are set as Enable or not. It shows "Updating……" during the upgrade. After upgrade, the equipment restarts and closes Update options as Disable automatically.

If you want to exit the menu when Update menu is still, you can only wait for automatic skip after 5 minutes or close the machine, then Update option will be Disable. Please select corresponding main and subordinate FPGA program!

If the power is off during updating, it returns to former vision before upgrade.

4.2 MVIO Delay Upgrade Introduction

4.2.1 Upgrade cable connection

3-pin cable, RS232 protocol Separately connected to DB15 of MVIO chassis and DB9 of computer.

Pin connection:

DB15：2-----DB9：2；DB15：3----DB9：3；DB15：5----DB9：5

4.2.2 Setup of Upgrade Program

The software for upgrade is ![RemoteUpdate.exe]. Please confirm that ![PCOMM.DLL 2.2.3.0 PComm DLL for Win32]

and ![RemoteUpdate.exe] are put in the same document. After that run the main upgrade software.

4.2.3 Usage of Upgrade Program

Connect MVIO DELAY to computer through serial port RS232, then use the special software on the computer for updating. Picture shows as:
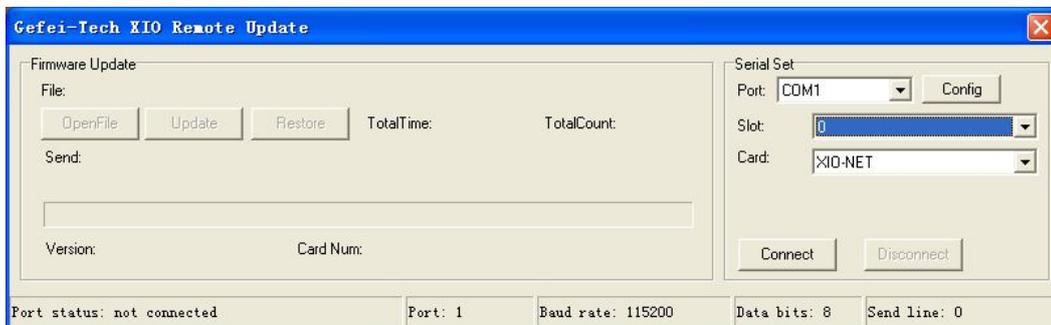
1. To confirm the connection between equipment and computer's serial port, open the software and select current serial port number at "Port". Usually it is com1. "Config" is used to set parameter of serial port, Usually you don't need to set it specially, but use the default setting. "Slot" should be 15. "Card" should be VIO DELAY-H (M) or VIO DELAY-H (S), which means upgrading inner corresponding main or subordinate program. Then click "Connect", and it shows the connection is successful.

2. After the correct connection, when the inner FPGA program is detected, "Restore" will light up. Then press this button to clear up original operations.

3. Click" OpenFile", select corresponding program for upgrade (please select the right main or subordinate FPGA program carefully!).

4. Click "Update". Several minutes later, it prompts the updating is successful.

5. After updating, the machine restarts automatically.

V MVIO Delay Technical Specification

Digital Video Input:

Input Interface: 1*SDI, BNC connection

Impedance: 75Ω

Format: SD: SMPTE 259M-C; 270Mb/s

HD: SMPTE 292M; 1.485Gb/s

Formate for self-adaptive:
SD: 525i60、625i50
HD: 720p60、720p59.94、720p50、1080i60、1080i59.94、
1080i50、1080p30、1080p29.97、1080p25

Return Loss: ＞15 dB，5MHz to 1.5GHz

Maximum cable length: SD: ＜200m (Belden 1694A)

HD: ＜100m (Belden 1694A)

Reference Input:

Signal Type: Anolog composite sync or tri-level sync

Input Interface: 1*CVBS / Tri-level, BNC

System: PAL/NTSC/Tri-level

Impedance: 75Ω

Digital Video Output:

Output Interface: 3*SDI, BNC connection

Impedance: 75Ω

Format: SD: SMPTE 259M-C; 270Mb/s

HD: SMPTE 292M; 1.485Gb/s

Return Loss: ＞15 dB，5MHz to 1.5GHz

Signal Level: 800mV±10%

Overshooting: ＜80mV

Jitter: ＜135ps (100KHz)

Rise and fall time: ＜270ps

Rise and fall time difference: ＜100ps

DC Level Shift: 0V±500mV

Control Interface:

Interface Type: 1* DB9，Female

Date Type: RS232

VI Service and Support

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